MEMORY DEVICE WITH COMMON ROW INTERFACE

Abstract

One embodiment of the present invention provides a semiconductor memory receiving an external address including an array address and a row address. The semiconductor memory includes a memory bank having N arrays, each array having an array address and a plurality of primary rows of memory cells and a plurality of redundant rows of memory cells, a redundancy block, and N local row control blocks. The redundancy block provides a match signal having an active state when the external address matches one of a plurality of defective addresses, provides a redundant row address when the match signal has the active state, and provides a redirected array address comprising a redundant array address when the match signal has the active state and otherwise comprising the external array address. Each of the N local row control blocks is associated with a different one of the N arrays, wherein the local row control block associated with the array whose address matches the redirected array address opens a redundant row of memory cells for access based on the redundant row address when the match signal has the first state, and otherwise opens a normal row of memory cells for access based on the external row address.